Atty. Dkt. No. 039153-0433 (C167596-CIP)

REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claims 19 and 20 are currently being amended.

This amendment adds, changes and/or deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claims remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 19-38 are now pending in this application.

As a preliminary matter, on page 2 of the Office Action, claim 19 is objected to for informalities. Applicants have amended claims 19 and 20 in accordance with the Examiner's suggestion. No new matter is added. Claims 19 and 20 are not amended in the limiting fashion. Withdrawal of the objection is respectfully requested.

On page 3 of the Office Action, claims 19-24 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,030,847 (Fazan). The Examiner states:

> Fazan et al. teaches an integrated circuit including at least one transistor, the integrated circuit comprising:
>
> A pair of local interconnects (65) spaced from each other by a minimum lithographic feature and each being a minimum lithographic feature (see figure 5); and
>
> A gate of the transistor (22) disposed in the space between the local interconnects and separated from of the local interconnects by an insulating liner (35, called spacer), wherein the space is less than or equal to the minimum lithographic feature, whereby the width of the transistor is not greater than three of the minimum lithographic feature (see figures 4-5).

> Regarding to claim 20, wherein the insulating spacers (35) are each disposed on an interconnect wall adjacent the gate to separate each of the local interconnects from the gate (see figures 4-5).
>
> Regarding to claim 22, the pair of local interconnect are space from each other by a minimum lithographic feature (see figures 4-5).

Applicants respectfully traverse the rejection. Applicants respectfully submit that Fazan clearly does not disclose each and every element of independent claims 19 and 21.

Claim 19 recites a pair of local interconnect spaced from each other by a minimum lithographic feature. The gates for FETs 22 of Fazan appear to be formed in a conventional lithographic process and are therefore no less than one minimum lithographic feature wide. There is no discussion in Fazan that such gates are fabricated at a size less than a lithographic feature. Figure 5 of Fazan does not disclose that each local interconnect (contact 65 under the Examiner's interpretation) are each a minimum lithographic feature. In fact, contacts 65 appear to be substantially larger than the minimum lithographic feature associated with gates of FETs 22. In addition, claim 19 recites that the space between the local interconnects is a minimum lithographic feature. Clearly, the space between contacts 65 is far more than one lithographic feature. Accordingly, one of ordinary skill in the art reading Fazan would clearly realize that Fazan does not disclose a pair of local interconnects being a minimal lithographic feature and a space between the local interconnects being less than or equal to the minimal lithographic feature. Therefore, independent claim 19 and its dependent claim 20 are patentable over Fazan.

Claim 21 is patentable for a similar reason to claim 19. Claim 19 recites that the space is less than or equal to a minimum lithographic feature. The space is for the gate of FET 22 is at least one lithographic feature. As shown in Figure 5 of Fazan, the space between what the Examiner interprets as local interconnects (contact 65) is substantially larger than the minimum lithographic feature. Indeed, two FETs 22 appear to be provided in the space between contacts 65. Applicants note that region 40 is an oxide layer and cannot possibly be considered a local interconnect. Accordingly, claim 21 and its dependent claims 22-24 are patentable over Fazan art.

On page 4 of the Office Action, claims 25-38 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,940,710 (Chung) in view of U.S. Patent No. 6,287,951 (Lucas). The Examiner states:

> Referring to figures 2a-2e, Chung et al. teaches an integrated circuit including at least a pair of local interconnects with one interconnect on each side of gate transistor, the integrated circuit being manufactured b a method comprising the steps of:
>
> Forming on a semiconductor substrate (1) a thick insulating layer (6);
>
> Forming at least a pair of space apart openings (30) in the insulating layer adjacent the semiconductor substrate (1);
>
> Forming a source (14) in one of the openings (30) and the drain (14) none of the openings;
>
> Filling each of the openings with a conductive material (8) to form the local interconnects (8), the local interconnect being electrically couple to the source and drain (14);
>
> Removing a portion of the insulating layer (6) to form a gate opening between the local interconnects (8);
>
> Forming a gate dielectric (4) on the semiconductor substrate (1) in the gate opening; and
>
> Forming the gate (5) on the gate dielectric layer.

Applicants respectfully traverse the rejection. Applicants traverse the rejection because Lucas is not prior art to present application.

The present application is a divisional of U.S. Patent Application No. 09/515,875, filed on February 29, 2000, which is a continuation-in-part application of U.S. Application No. 09/119,934, filed on July 21, 1998 (the parent application) (U.S. Patent No. 6,146,954). Support for claim 25 is found in the parent application in the detailed description on pages 7, lines 18-24 and in Figures 10 and 14. The filing date of the parent application is well before the filing date

of Lucas. Therefore, Lucas does not qualify as prior art. Accordingly, withdrawal of the rejection of claims 25-38 is respectfully requested.

Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. § 1.136 and authorize payment of any such extensions fees to Deposit Account No. 06-1447.

Respectfully submitted,

Date 11-03-04

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